CDB4228A

Evaluation Board for CS4228A

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives AES/EBU, S/PDIF & EIAJ-340 compatible digital audio
- CS8404 transmits AES/EBU, S/PDIF & EIAJ-340 compatible digital audio
- PC software provides easy to use board and device control
- Interfaces for external serial audio I/O and microprocessor control

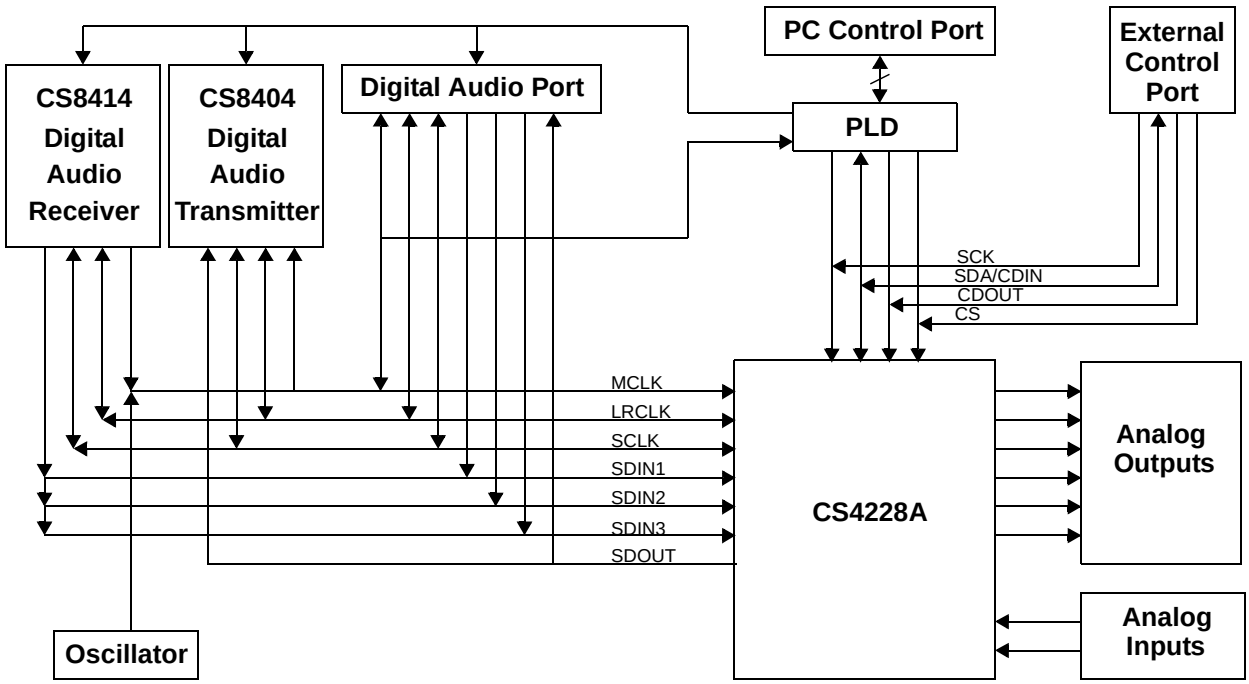
Description

The CDB4228A evaluation board is an excellent means for quickly evaluating the CS4228A 2 in, 6 out, 24-bit, 96kHz capable CODEC. Evaluation requires an analog signal source and analyzer, a digital signal source and analyzer, a PC compatible computer for control, and a power supply.

System timing can be supplied by the CS8414 digital audio receiver I.C., or an onboard oscillator. Control is provided by PC software. The evaluation board may also be configured to accept external timing, data, and control signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4228A	Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/sales/cfm

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1. CDB4228A SYSTEM OVERVIEW

The CDB4228A evaluation board is an excellent means of quickly evaluating the CS4228A. Input and output analog interfaces are provided as well as a CS8414 digital interface receiver and CS8404 digital interface transmitter that provide an easy interface to digital audio test equipment. The evaluation board also allows the user to interface external systems' digital audio clocks and data through the digital audio port (DAP) 20-pin header. An external two wire or SPI control interface is also provided through a 10-pin header for easy system development using the evaluation board.

The CDB4228A schematic has been partitioned into 17 schematics shown in Figures 1 through 17. Each partitioned schematic is represented in the top level schematic shown in Figure 1.

2. CS4228A CODEC

A complete description of the CS4228A CODEC is included in the CS4228A data sheet.

3. BOARD CONTROL

3.1 Graphical User Interface

The CDB4228A is shipped with Windows based graphical user interface (GUI) software for interfacing with the CS4228A control port via a PC parallel port connected to the DB25 connector, J15. Parallel port control is selected by placing the CONTROL switch S2 in the PP position. The software can be used to communicate with the CS4228A in two wire or SPI mode by selecting the MODE switch S4. Further documentation for the software is available on the distribution diskette in the plain text format file, README.TXT.

3.2 External Control Interface

The evaluation board can also be controlled via a external host such as a microcontroller connected to the EXTRNL CONTROL port JP9 by placing the CONTROL switch S2 in the EXTRNL position. For more information, see section 7.

4. DIGITAL AUDIO I/O

4.1 Receiver

Digital-to-Analog (DAC) performance can be quickly tested by connecting a S/PDIF audio source to the CS8414 receiver. The S/PDIF input can be either optical or coax, see Figure 16. However, both inputs cannot be driven simultaneously. The interface for the CS8414 includes a serial bit clock, serial data, left-right clock (FSYNC), and a 256 Fs master clock. The bit clock and left-right clock signals are bidirectional, and as a pair can be selected to supply these signals to the system, or can be selected as inputs from the CS4228A or DAP. The receiver data output can be simultaneously connected to the SDIN1, SDIN2, and SDIN3 inputs on the CS4228A.

The receiver can be powered down to prevent asynchronous clock interference by depressing all three rocker switches to the OFF position on the RX PWR DIP switch S1.

The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 data sheet.

4.2 Transmitter

The analog-to-digital converter performance can be quickly evaluated by connecting an analog generator to the left and right inputs, and connecting the S/PDIF optical or coaxial output to audio test equipment. The CS8404 digital interface transmitter is connected to the CODEC serial data output SDOUT, and the system bit clock, left-right clock and master clock as shown in Figure 17. The transmitter and CS4228A share several serial modes, but not all modes of each device are supported. SMODE 4 and 5 will not work properly with the transmitter: The data will be right-shifted by 8 bits.

The transmitter must always be supplied a 128 Fs master clock, which is supplied by clock dividers within the PLD. The clock divider source is the same as that selected for the CS4228A MCLK. The

PLD can support division ratios of 1, 2, 3, and 4 to support MCLK frequencies of 128, 256, 384, and 512 Fs respectively. The proper division ratio can be selected in the GUI in PP mode, or S5 in EXTRNL mode.

4.3 Digital Audio Port

The digital audio port (DAP) provides an interface to the CODEC serial audio clocks and data. The DAP can be used to interface to external compressed audio decoder systems such as the CS492x or CS49300 families of digital signal processors for ease in evaluating complete audio system solutions. MCLK, LRCLK, and SCLK are bidirectional signals. The direction of these signals can be controlled by the GUI in PP mode, or S5 switches in EXTRNL mode. The direction of SCLK and LRCLK is always selected as a pair.

4.4 Master Clock

Master clock (MCLK) for the evaluation board can come from one of three sources: the on-board CS8414 receiver, the on-board oscillator, or an external source via the DAP port. One of the three sources is selected by multiplexer U2 which is controlled via the GUI in PP mode or the S5 switches in EXTRNL mode. The on-board oscillator provided with the board is 12.288 MHz for evaluation at 256 Fs at a 48kHz sample rate, or 128 Fs at a 96kHz sample rate. The oscillator is socketed for easy replacement and can be powered down with header JP1 to prevent asynchronous clock interference when the S/PDIF receiver is being used.

The MCLK multiplexer adds a small amount of clock jitter to the MCLK signal, which has a very slight effect on converter performance. The system can be evaluated without the buffer by installing a 3x2 pin header in JP2, and removing R3. A 2-socket shorting jumper is then installed in JP2 to select the system MCLK source. Refer to Figure 15.

4.5 Serial Data Format

The serial data format for the evaluation board is set by the GUI in PP mode or by S5 switches in EXTRNL mode. Not all serial modes of each device are supported. SMODE 4 and 5 are not supported by the transmitter. Two serial formats are common to all three devices; I2S, 16 to 24 bits/sample, and right justified, 16 bits/sample.

Each of the three SDIN inputs to the CS4228A comes from a multiplexer within the PLD and can be individually sourced from the CS8414 receiver or from the DAP. The multiplexer can be disabled and jumpers JP3-JP5 can be used to select the source.

5. ANALOG INPUT

Analog inputs to the CDB4228A are single ended, with a full scale of 2V RMS (5.66V p-p). The inputs are AC coupled, then converted to a differential signal with a 2.3V common mode voltage derived from the 5V supply. The differential signal is then anti-aliased with a passive filter, Fc = 200 kHz, before being sent to the ADC as shown in Figure 2.

6. ANALOG OUTPUT

The analog outputs from the DACs are buffered with a 2-pole active butterworth filter, Fc = 50 kHz. The filter has a DC gain of 1.56V/V for a 2V RMS full scale output. For a lower cost alternative, the outputs can be filtered with a single pole passive filter with Fc = 50 kHz and RL > 10k ohms as shown in Figure 11. The outputs also have a mute circuit that is controlled by the MUTEC pin on the CS4228A.

7. EXTERNAL CONTROL MODE

The CDB4228A system can be controlled without using a PC by connecting a host controller to the EXTRNL CTRL port. All board functions set by the parallel port are available to the user on the 10 position DIP switch, S5. There are three parameters on S5; board level serial mode, MCLK multiplexing, and S/PDIF transmitter clock divider control. On S5, an open switch denotes a one for that bit position.

7.1 Serial Mode

The SMODE[4..0] switches on S5 set the serial mode and the LRCLK/SCLK direction of all other devices in the system except the CS4228A. The devices controlled by SMODE include the CS8414, the CS8404, and the DAP. SMODE settings on S5 are only active when in EXTRNL mode. The SMODE mapping is shown in Table 1. Care must be taken when setting up SMODE so that the LRCLK/SCLK direction corresponds with the CS4228A master/slave setting to avoid bus contention. The CS4228A serial port master/slave mode is set in the Serial Port Mode register 0x0D.

7.2 MCLK Multiplexer

The board level MCLK source is controlled by the MCLK-SEL[2..0] switches on S5 when in EXTRNL mode. The multiplexer settings are shown in Table 3. The MCLK source should be the CS8414 whenever the S/PDIF data source is used.

7.3 Transmitter Clock Divider

The TX_MCLK[1..0] switches on S5 control the clock divider for the CS8404 S/PDIF transmitter when in EXTRNL mode. The transmitter must be supplied a 128 Fs MCLK which is sourced from the CS4228A MCLK multiplexer. The clock divider ratios are shown in Table 5.

8. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (+5V, GND, +12V, -12V). The +5V input supplies power to the analog and digital +5 Volt circuitry and to a 3.3V voltage regulator. There is a power supply header for selecting either 5V or 3.3V supplies to the CS4228A VL pin. A second header selects the interface voltage for the programmable logic device that supplies the control port interface. The VL setting should always be equal or greater than the PLD PWR to prevent noise due to charge injection.

9. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4228A requires careful attention to power supply and grounding arrangements to optimize performance. The decoupling capacitors are located as close to the CS4228A as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yields large reductions in radiated noise.

SMODE [4..0]	Board Level Serial Mode	CS8414 MODE	CS8404 MODE	DAP CLK MODE	CS8414 M[3..0]	CS8404 M[2..0]
0	I2S, TX Master, 64Fs SCLK only	Output	Input	Input	2	4
1	I2S, CODEC Master	Input	Input	Input	3	4
2	I2S, DAP Master	Input	Input	Output	3	4
3	Right Justified, TX Master, 16 bits	Output	Input	Input	5	5
4	Right Justified, CODEC master	Input	OFF	Input	15	4
5	Right Justified, DAP master	Input	OFF	Output	15	4
6	Left Justified, CODEC master	Input	OFF	Input	15	1
7	Left Justified, DAP master	Input	OFF	Output	15	1
8	Left Justified, test mode	Output	Input	Input	0	1
9	Left Justified, test mode	Input	Output	Input	1	0
10 - 31	I2S, CODEC master	Input	Input	Input	3	4

Table 1. Board Level Serial Mode Settings

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 Volt power
+12V, -12V	Input	+ 12/-12V Volt power for the op-amps
GND	Input	Ground connection from power supply
J9, SPDIF IN	Input	Digital audio interface input via coax
U9, SPDIF IN	Input	Digital audio interface input via optical
LEFT	Input	Analog audio input, 2V RMS (5.65Vp-p) full scale
RIGHT	Input	Analog audio input, 2V RMS (5.65Vp-p) full scale
DAC1 - DAC6	Output	Analog audio output, 2V RMS (5.65Vp-p) full scale
J7, SPDIF OUT	Output	Digital audio interface output via coax
U5, SPDIF OUT	Output	Digital audio interface output via optical
Parallel Port	Input/Output	Parallel connection to PC for two wire® or SPI control port signals
EXT CTRL	Input/Output	I/O for two wire® or SPI control port signals
DAP	Input/Output	I/O for serial audio clocks and data
PGM	Input/Output	Programming header for PLD

Table 2. System Connections

MCLK-SEL [2..0]	MCLK Source	DAP MCLK DIR
0	Oscillator	OFF
1	Oscillator	Output
2	S/PDIF Receiver	OFF
3	S/PDIF Receiver	Output
4	DAP	Input
5	None	OFF
6	None	OFF
7	None	OFF

Table 3. MCLK Multiplexer Settings

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
VD	Selects the supply voltage for the CS4228A digital core.	3.3V* 5V	
VL	Selects the supply voltage for the CS4228A logic interface pins	3.3V 5V*	
RX PWR	Selects the supply voltage for the Altera PLD I/O pins.	3.3V 5V*	
OSC PWR	Connects power to the oscillator	ON* OFF	
S1	Connects power and clocks to the CS8414	ON* OFF	Power and LRCLK and SCLK are connected Power, LRCLK, and SCLK are disconnected
S2	Selects control port interface	PP* EXTRNL	Parallel port control enabled. EXTRNL CTRL header enabled
S3	Selects the CS4228A SDIN1,2,3 source in EXTRNL control mode	SPDIF* DAP	CS8414 data is routed to SDIN1,2,3 SDIN1,2,3 source is the DAP
S4	Selects the control port data format	Two wire* SPI	Two wire control format SPI control format
S5	Selects serial mode and DAP clock directions in EXTRNL control mode.	CLOSED* OPEN	See external control mode section for more information.
JP2	Optional pin header select for MCLK	OSC SPDIF MCLK MUX MCLK	MCLK source is onboard oscillator. MCLK source is CS8414 receiver MCLK source is multiplexer

Notes: *Default setting from factory

Table 4. CDB4228A Jumper and Switch Settings

TX-MCLK [1..0]	MCLK Division Ratio	System MCLK Rate
0	1:1	128
*1	1:2	256
2	1:3	384
3	1:4	512

Table 5. Transmitter Clock Divider Settings

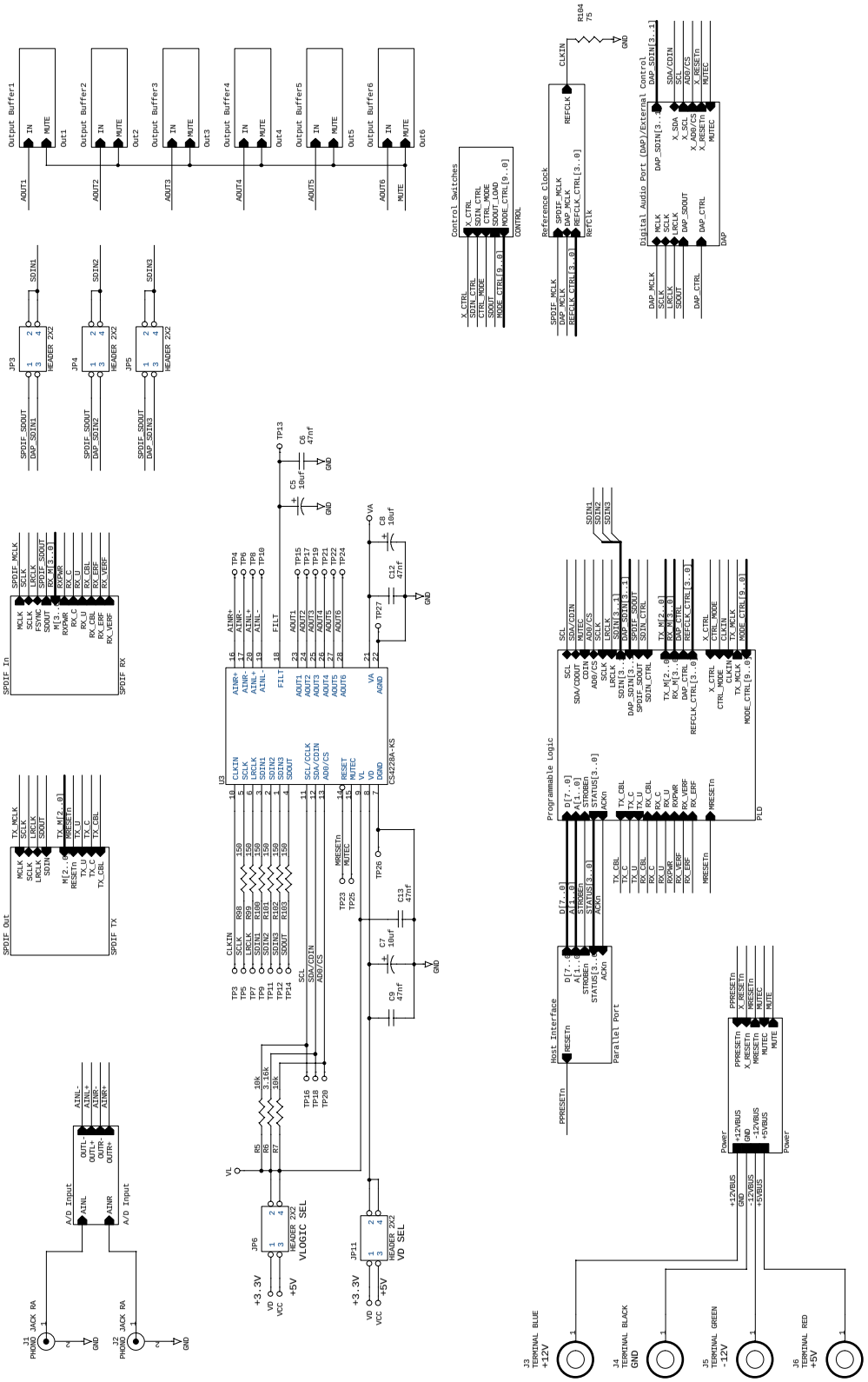

Figure 1. CDB4228A Top Level Schematic

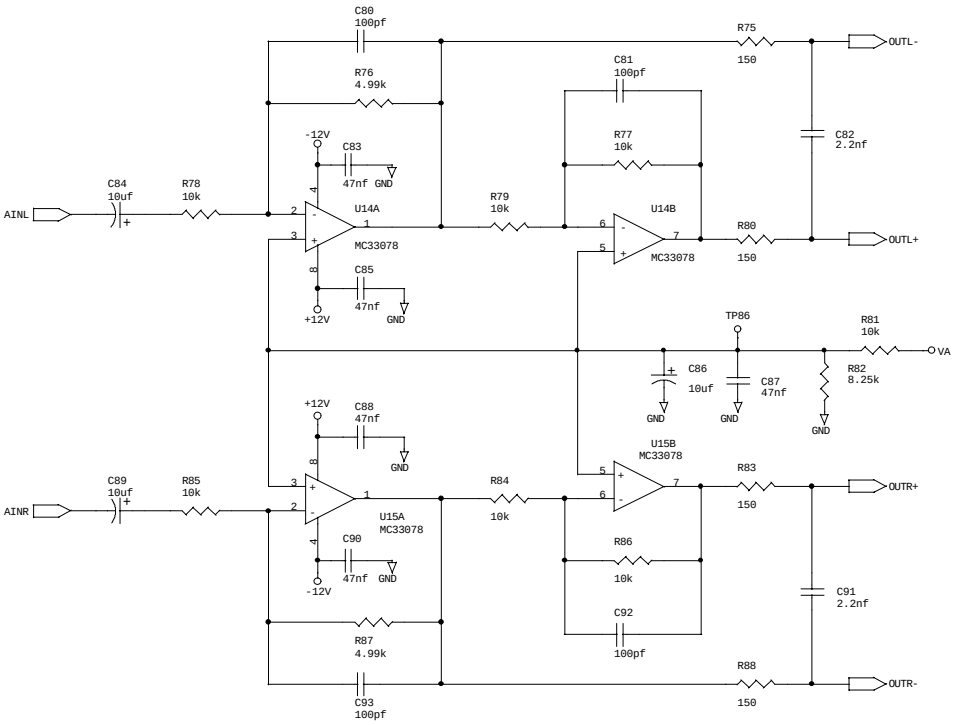

Figure 2. Analog Input Filter

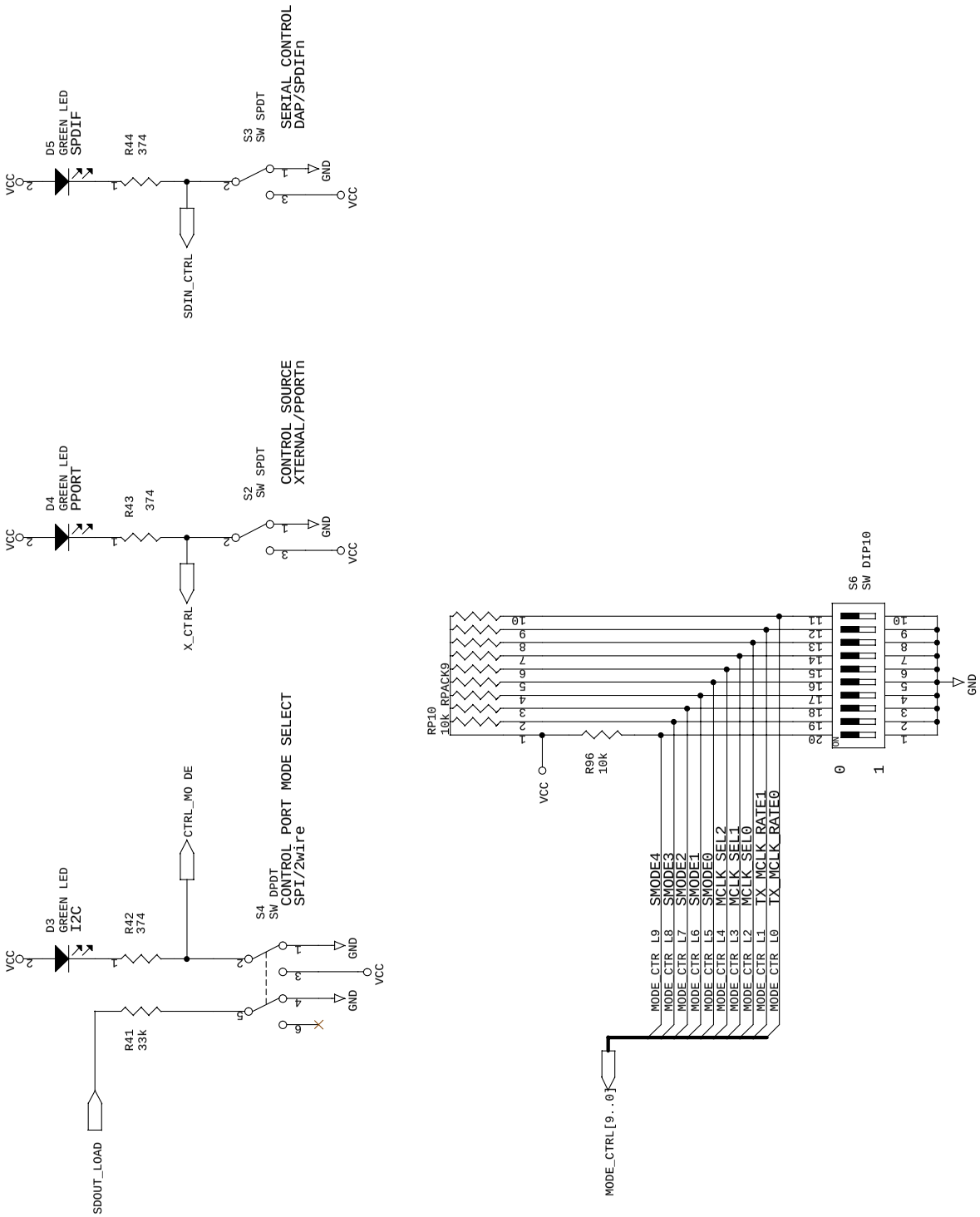

Figure 3. External Control

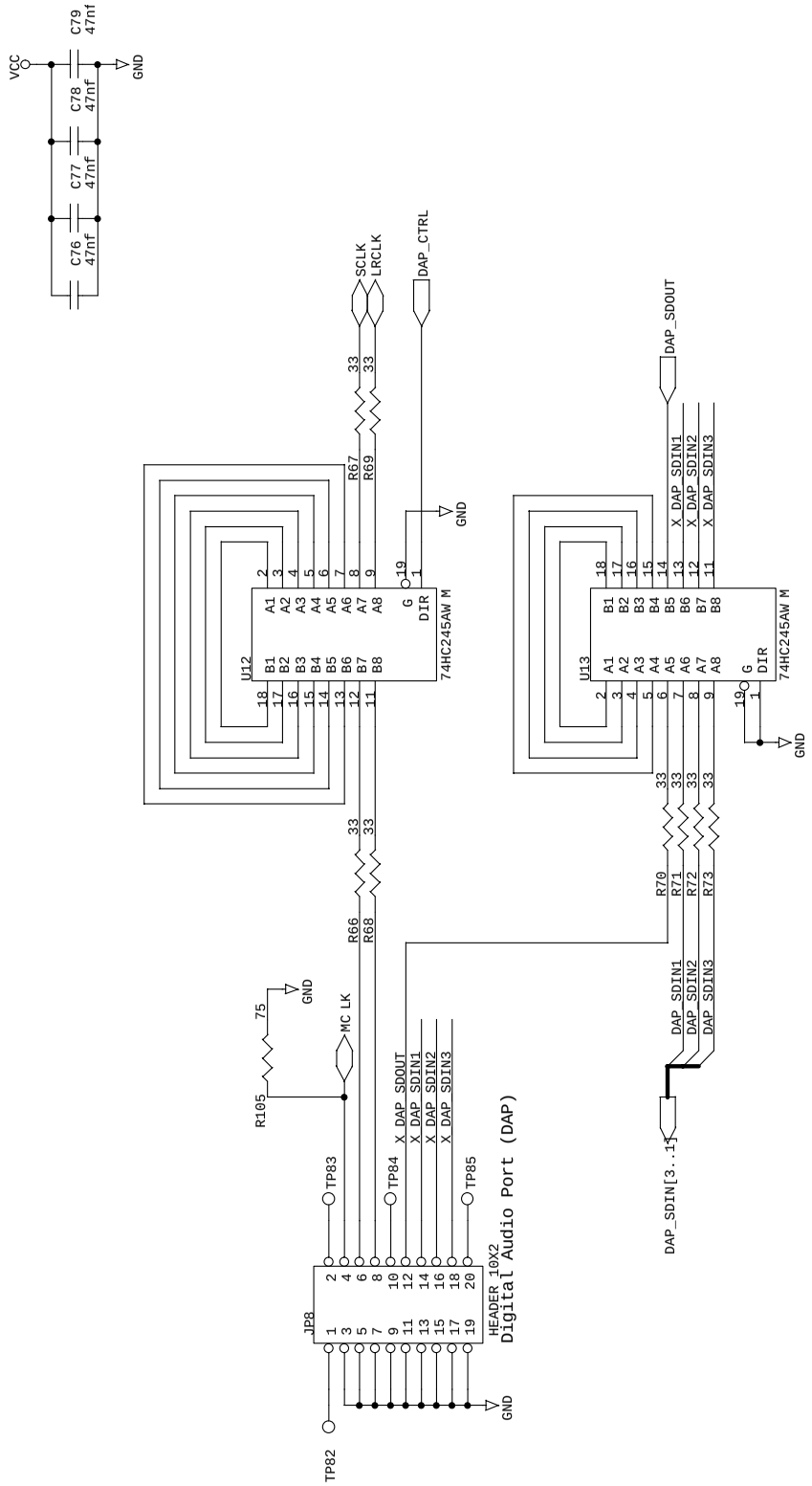

Figure 4. Digital Audio Port

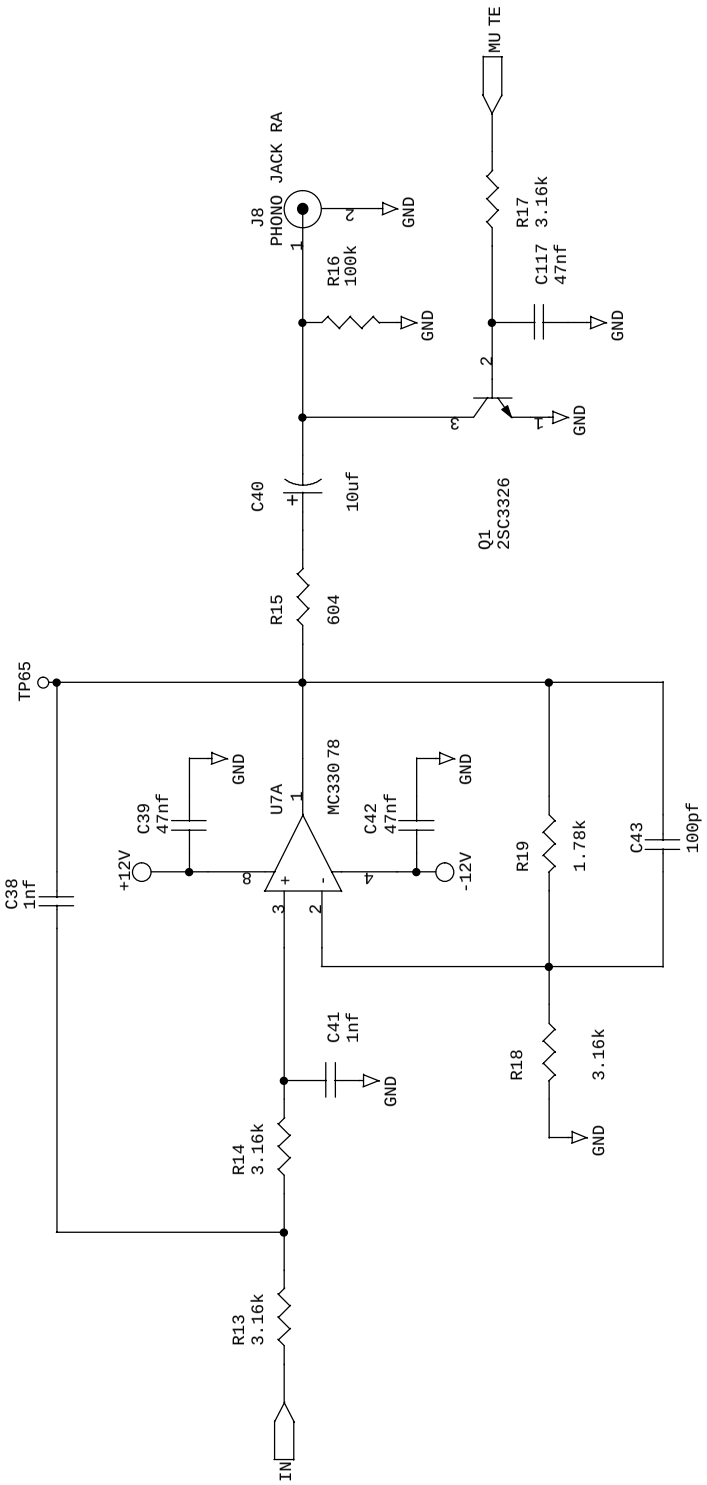

Figure 5. Analog Output Filter 1

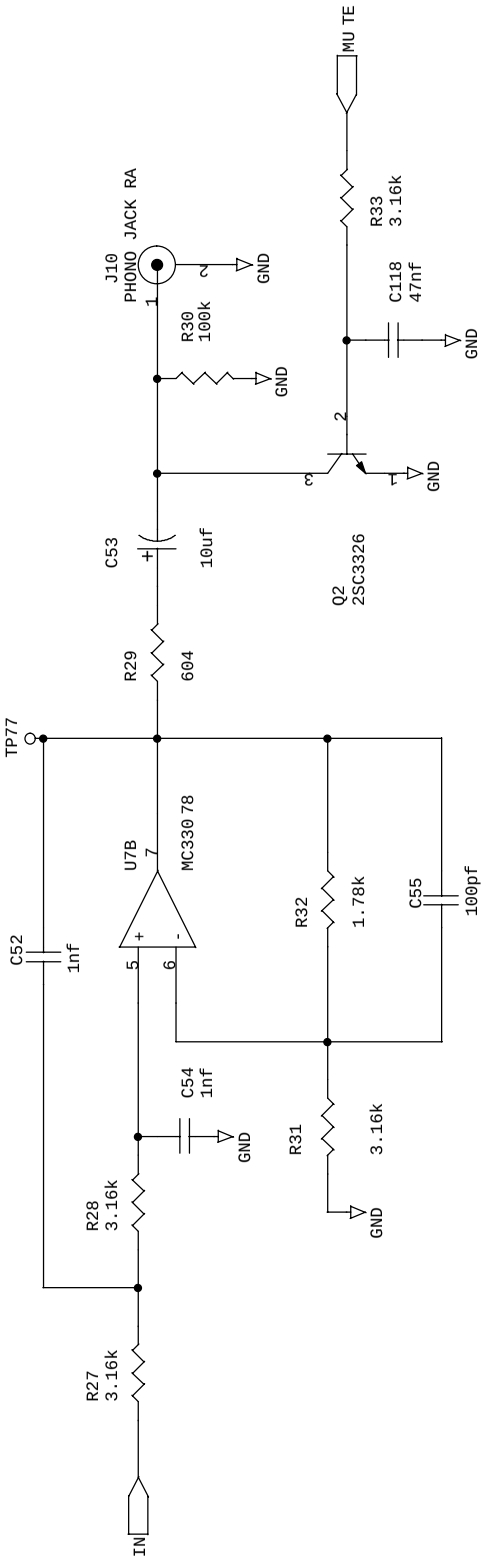

Figure 6. Analog Output Filter 2

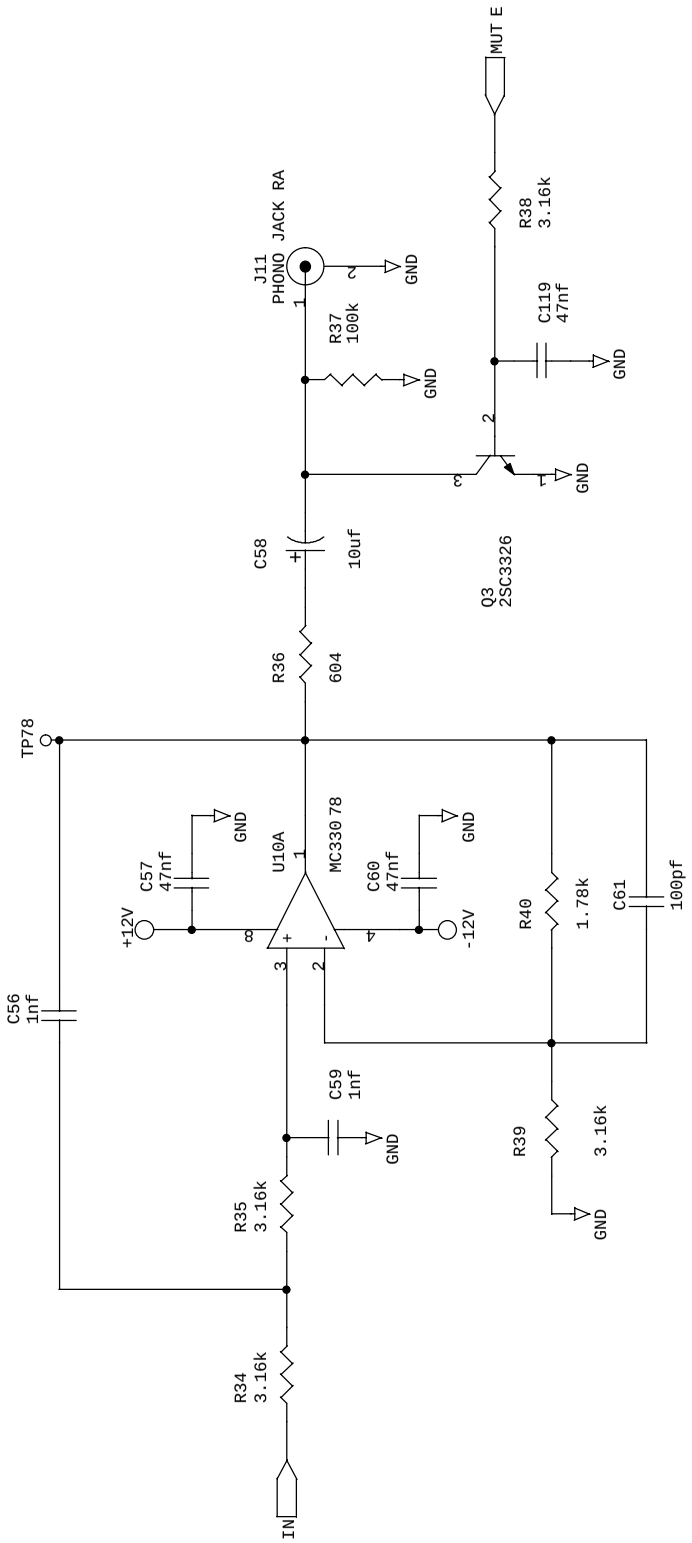

Figure 7. Analog Output Filter 3

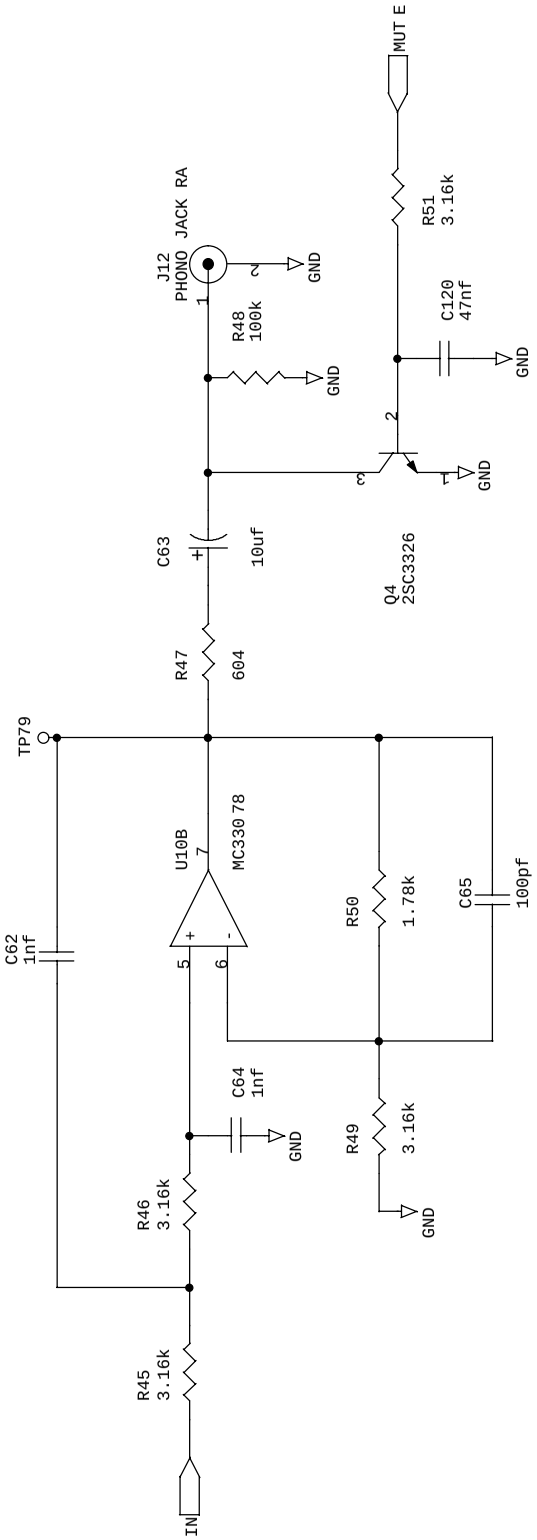

Figure 8. Analog Output Filter 4

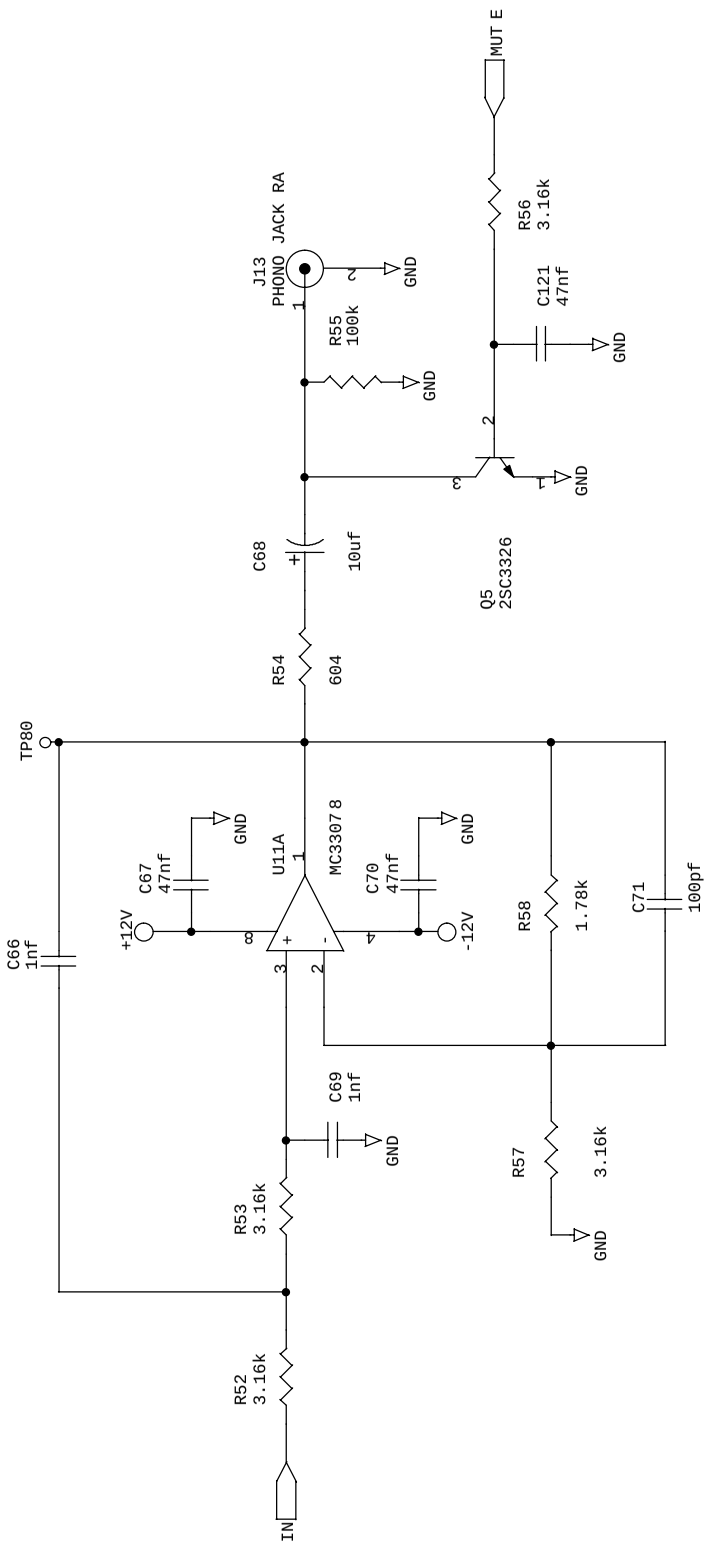

Figure 9. Analog Output Filter 5

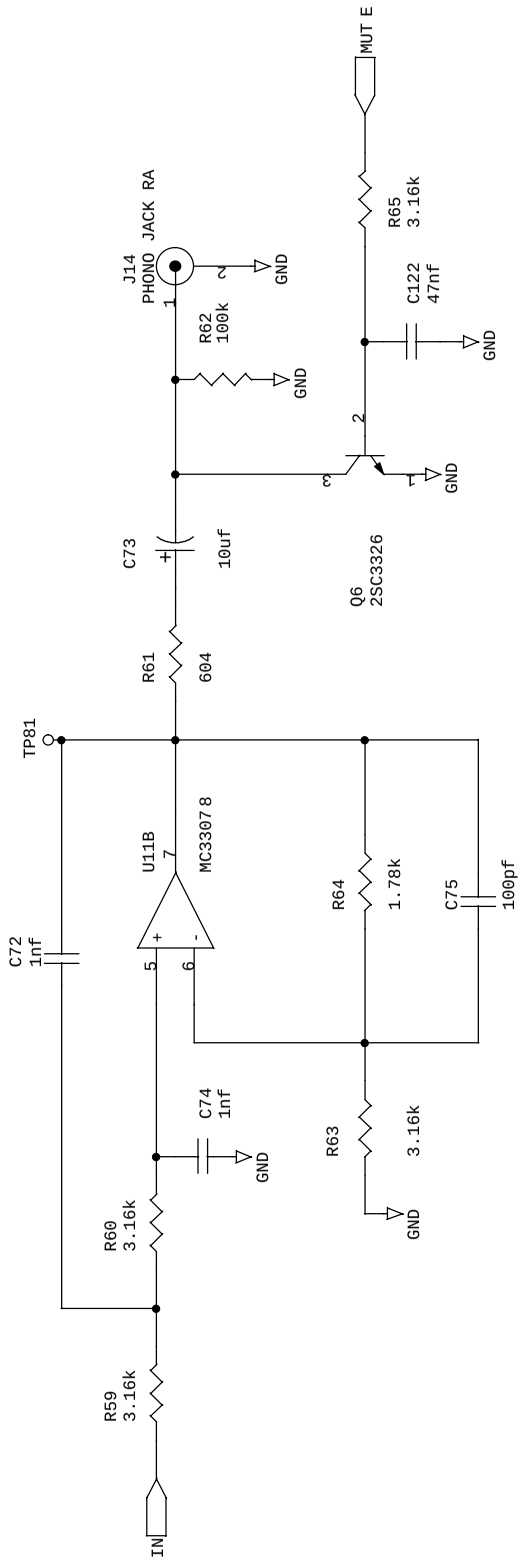

Figure 10. Analog Output Filter 6

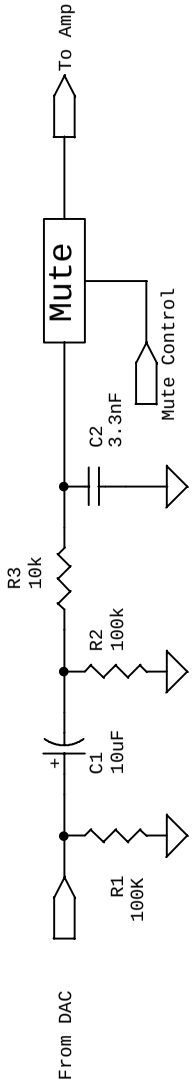

Figure 11. Low Cost Analog Output Filter

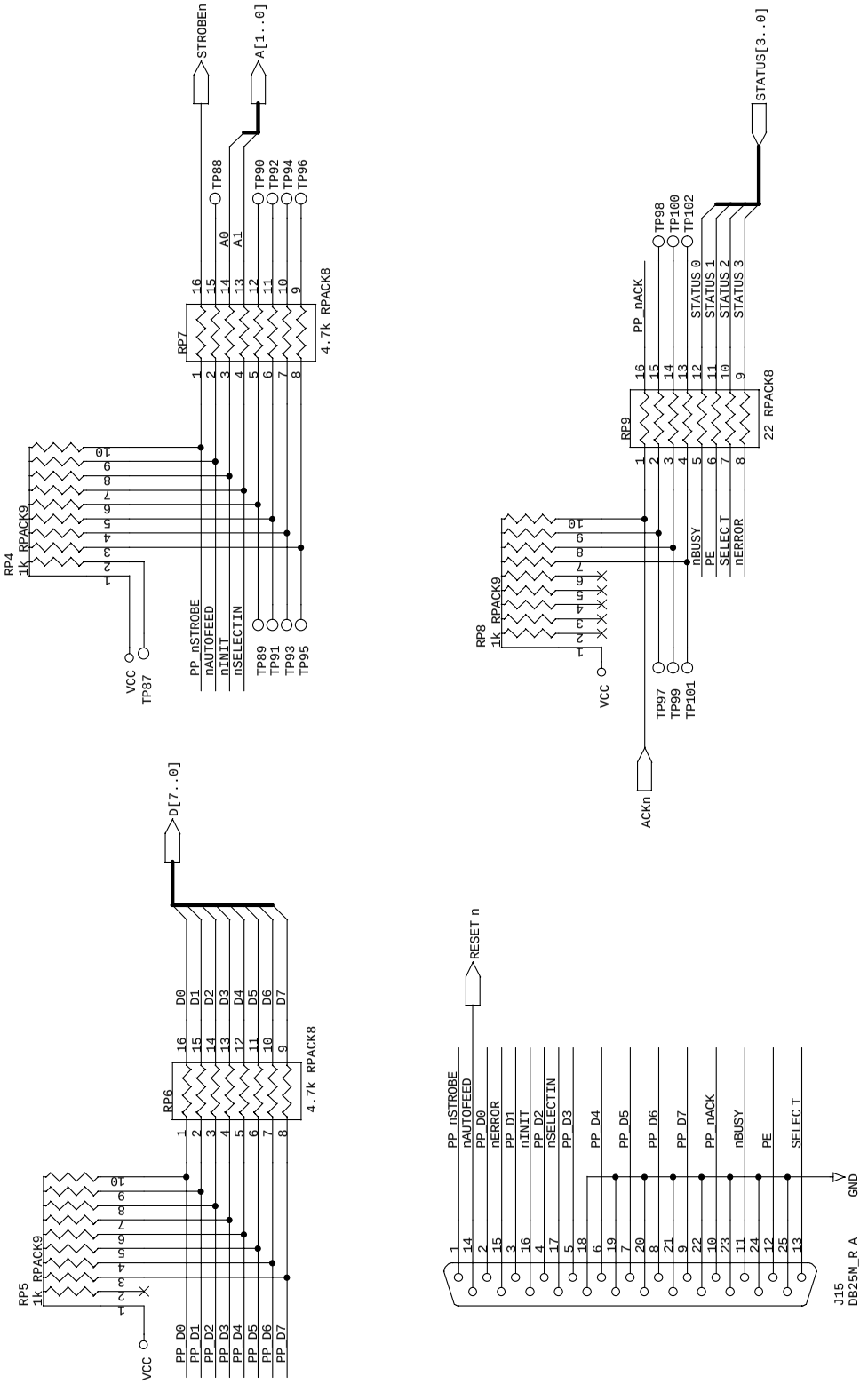

Figure 12. Control Port Interface

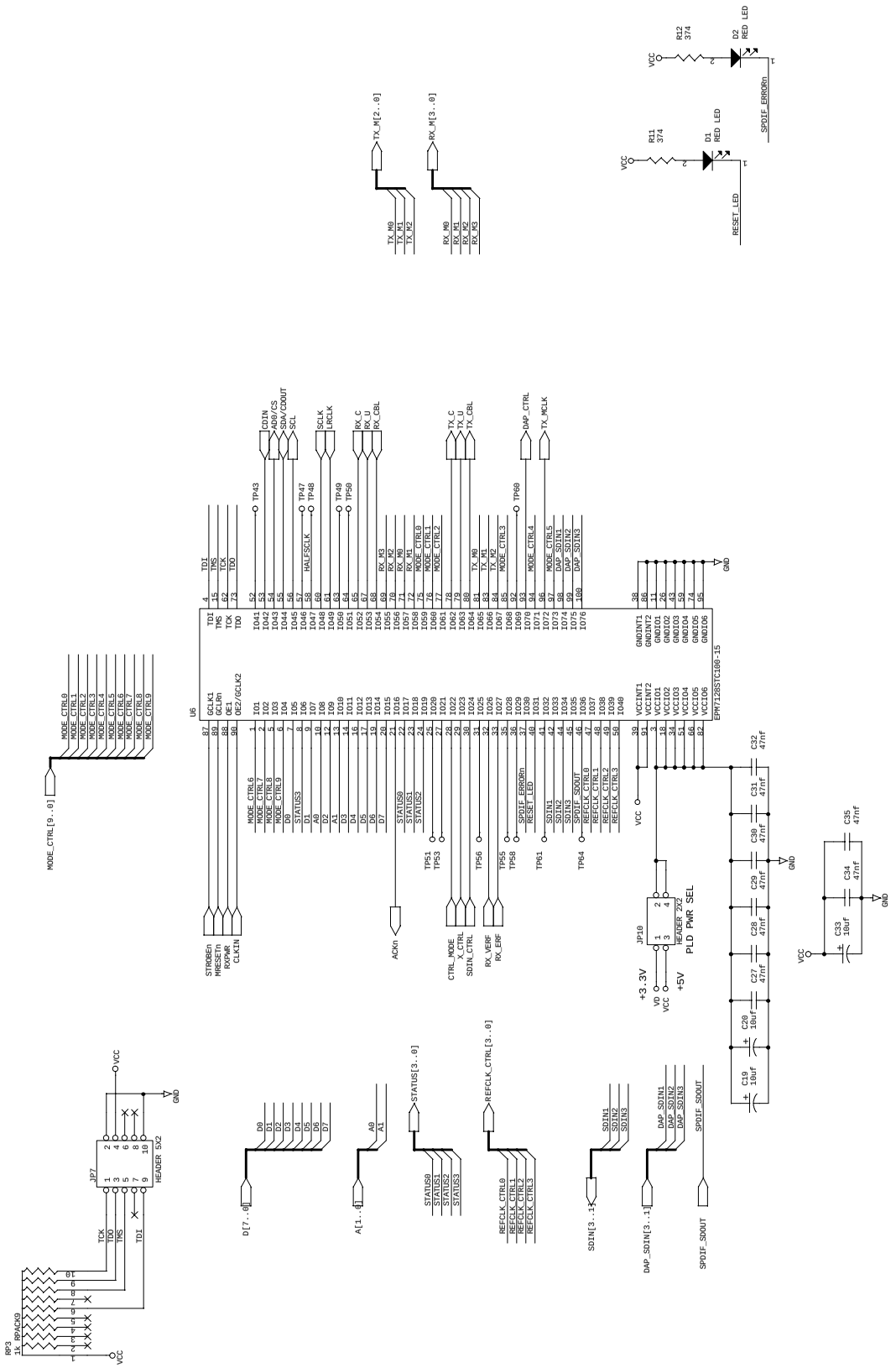

Figure 13. Programmable Logic

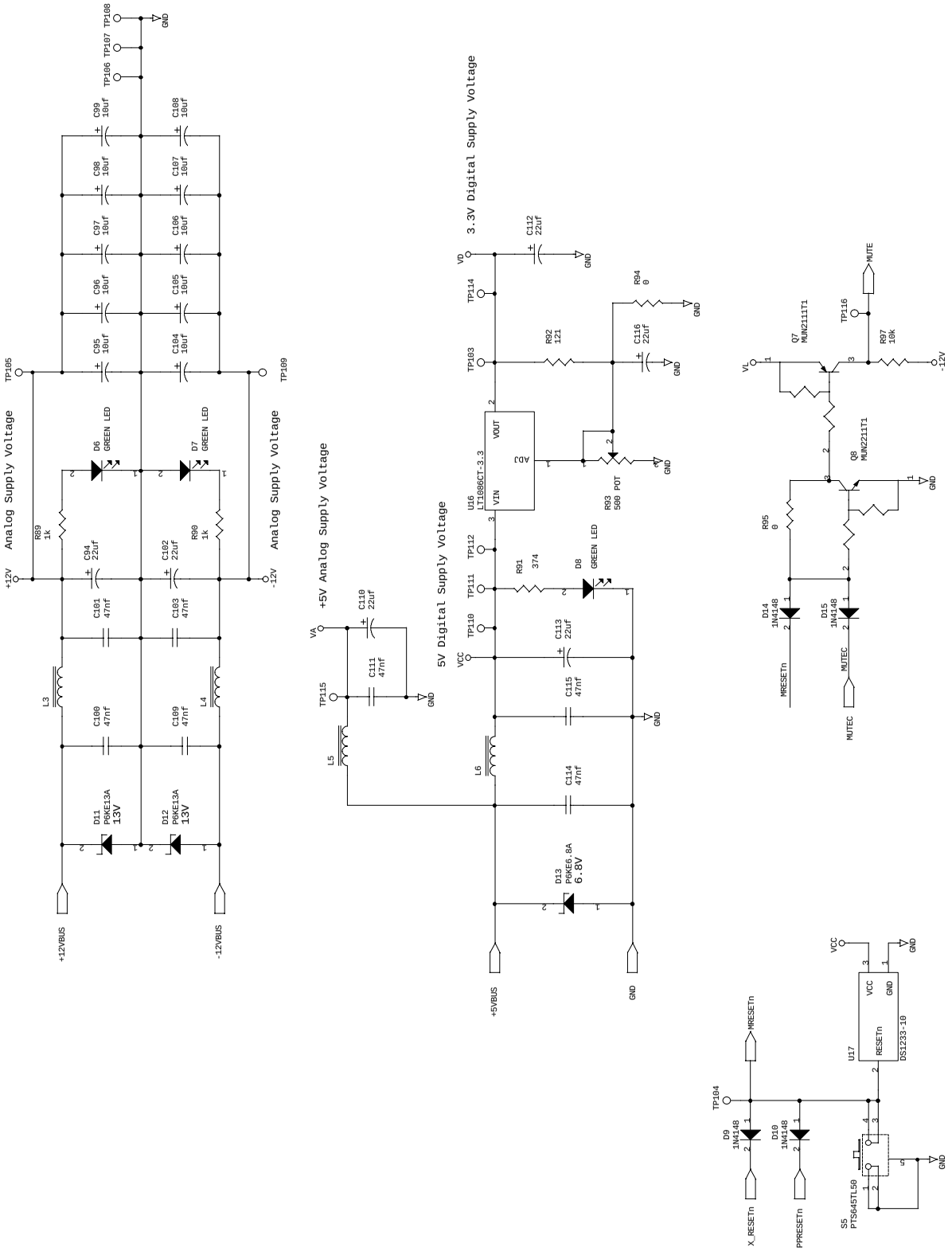

Figure 14. Power Supply

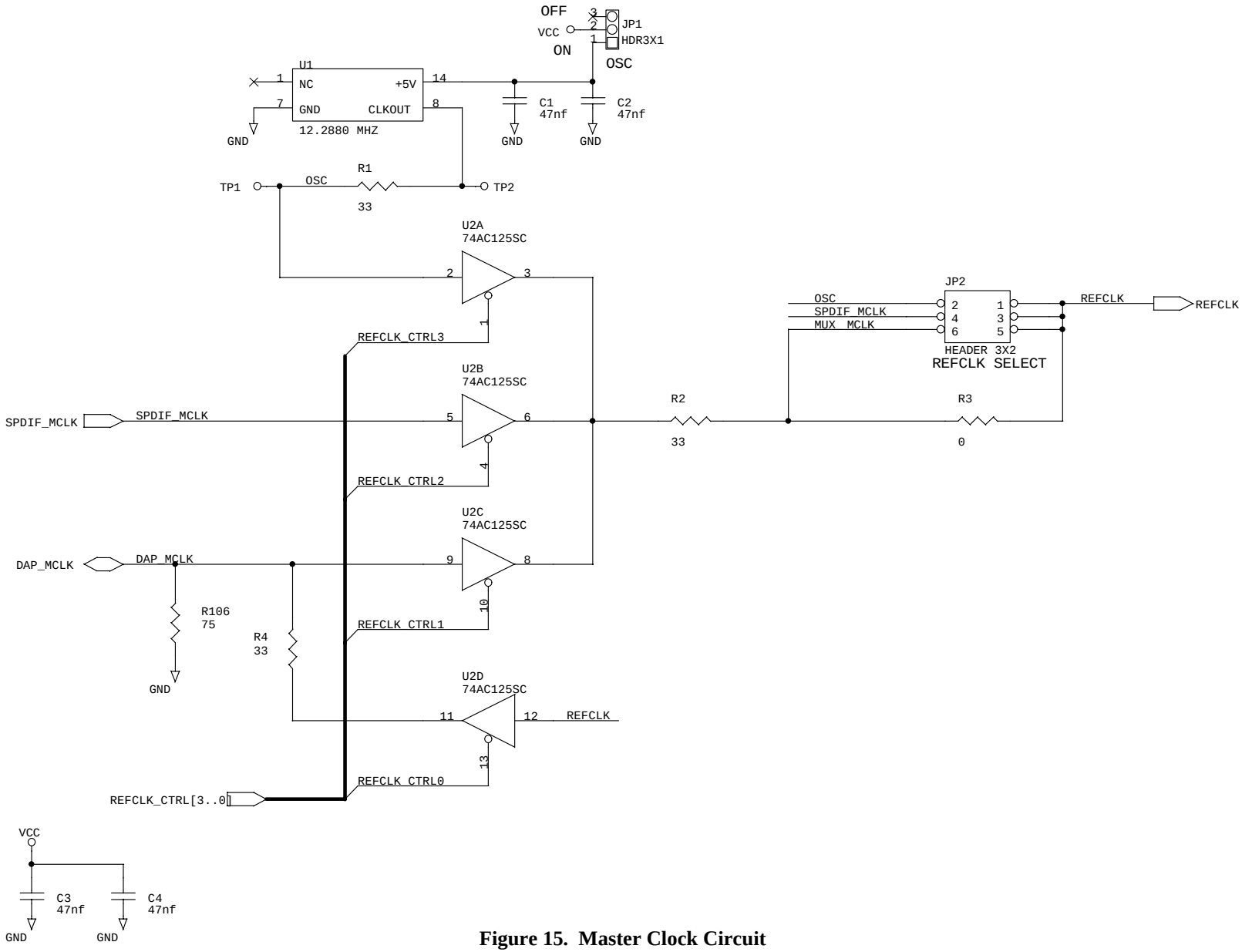

Figure 15. Master Clock Circuit

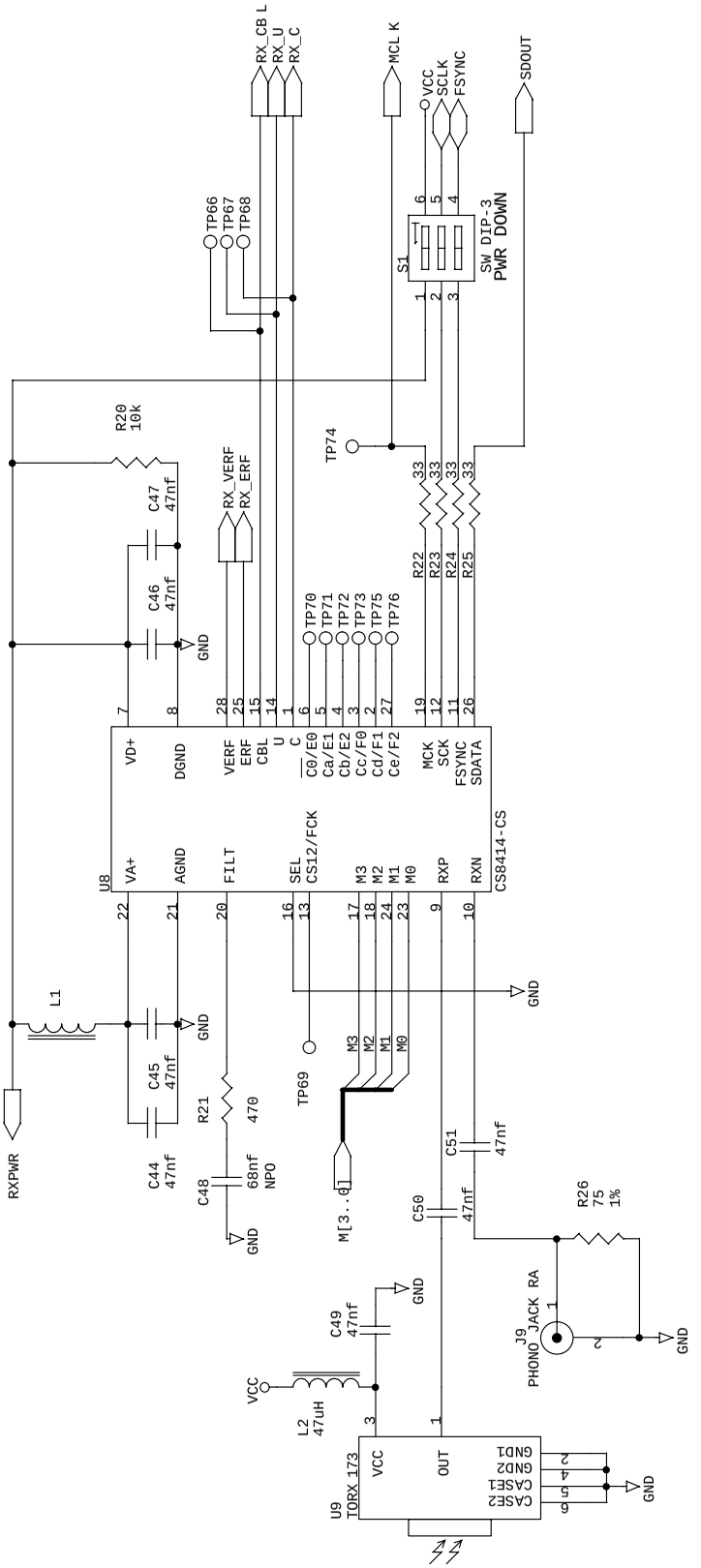

Figure 16. CS8414 Digital Audio Receiver

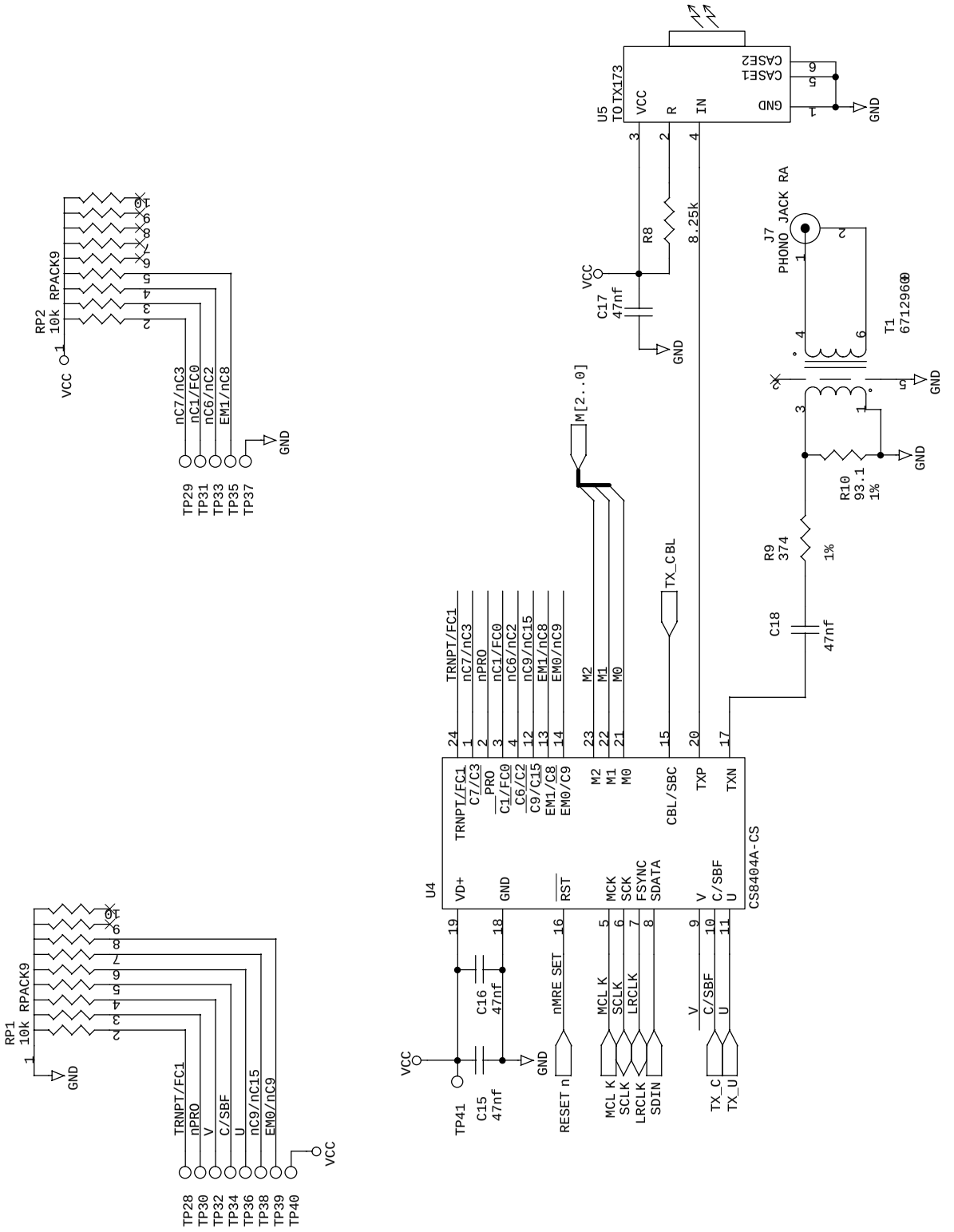

Figure 17. CS8404 Digital Audio Transmitter

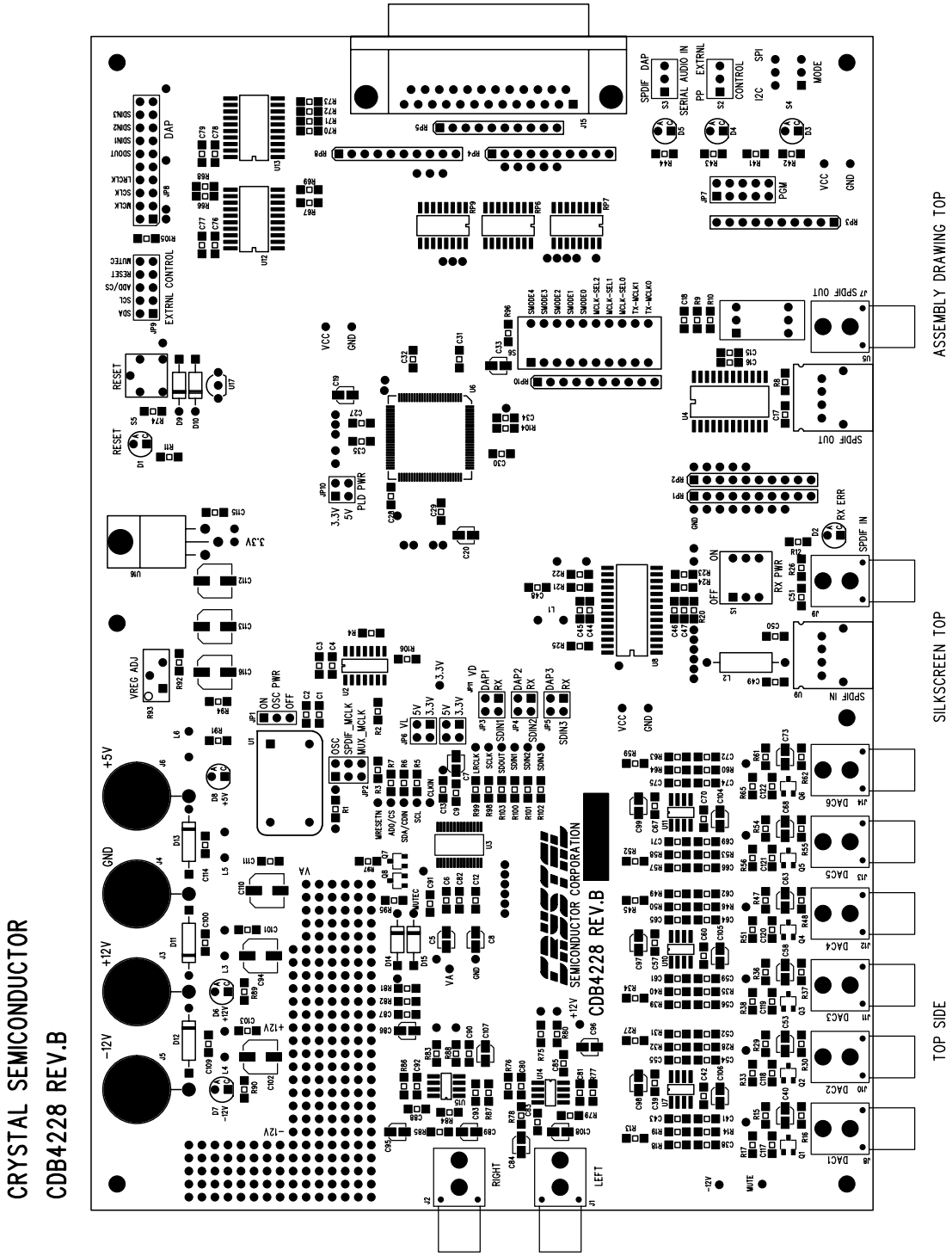

Figure 18. Silkscreen Top

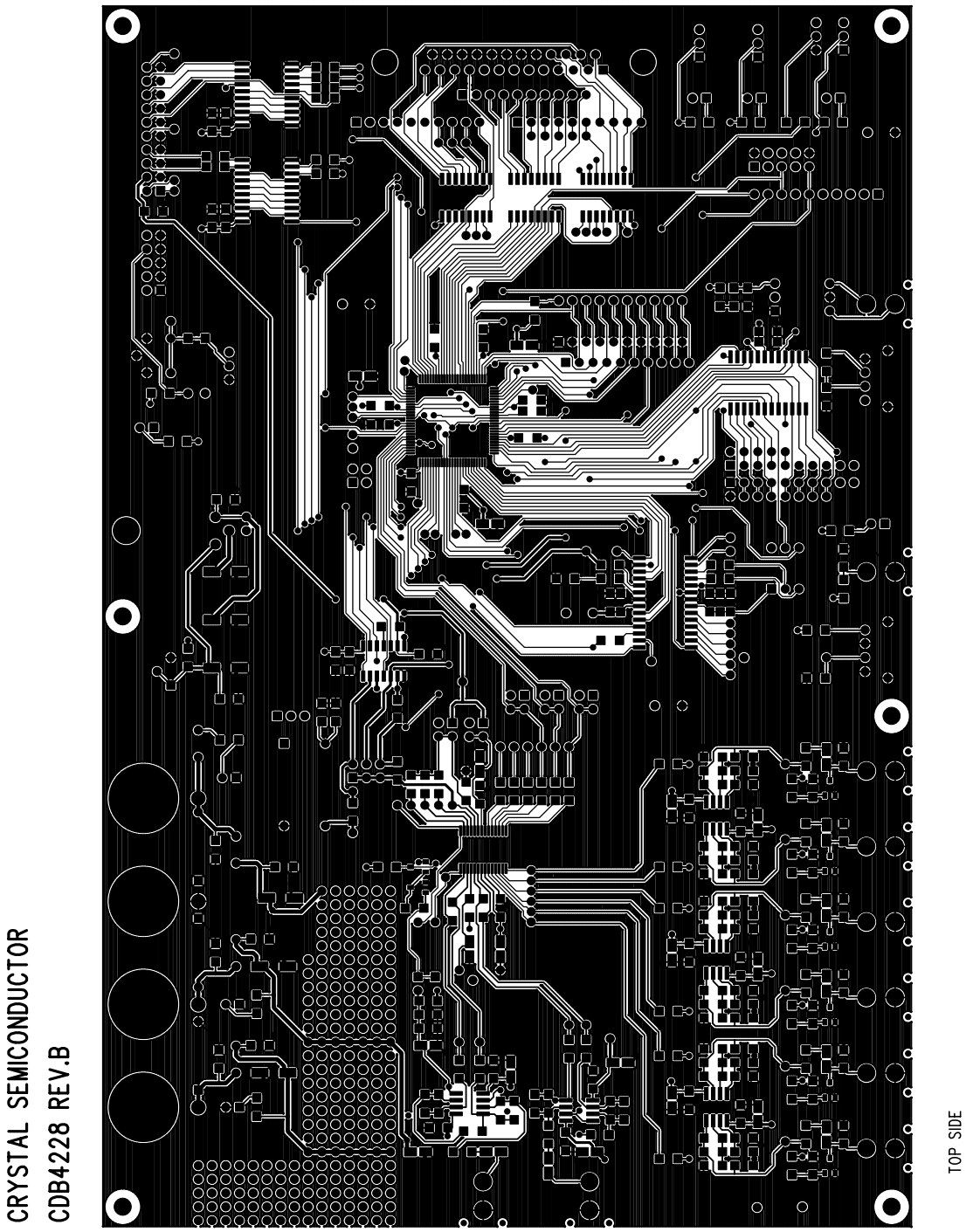

Figure 19. Top Side

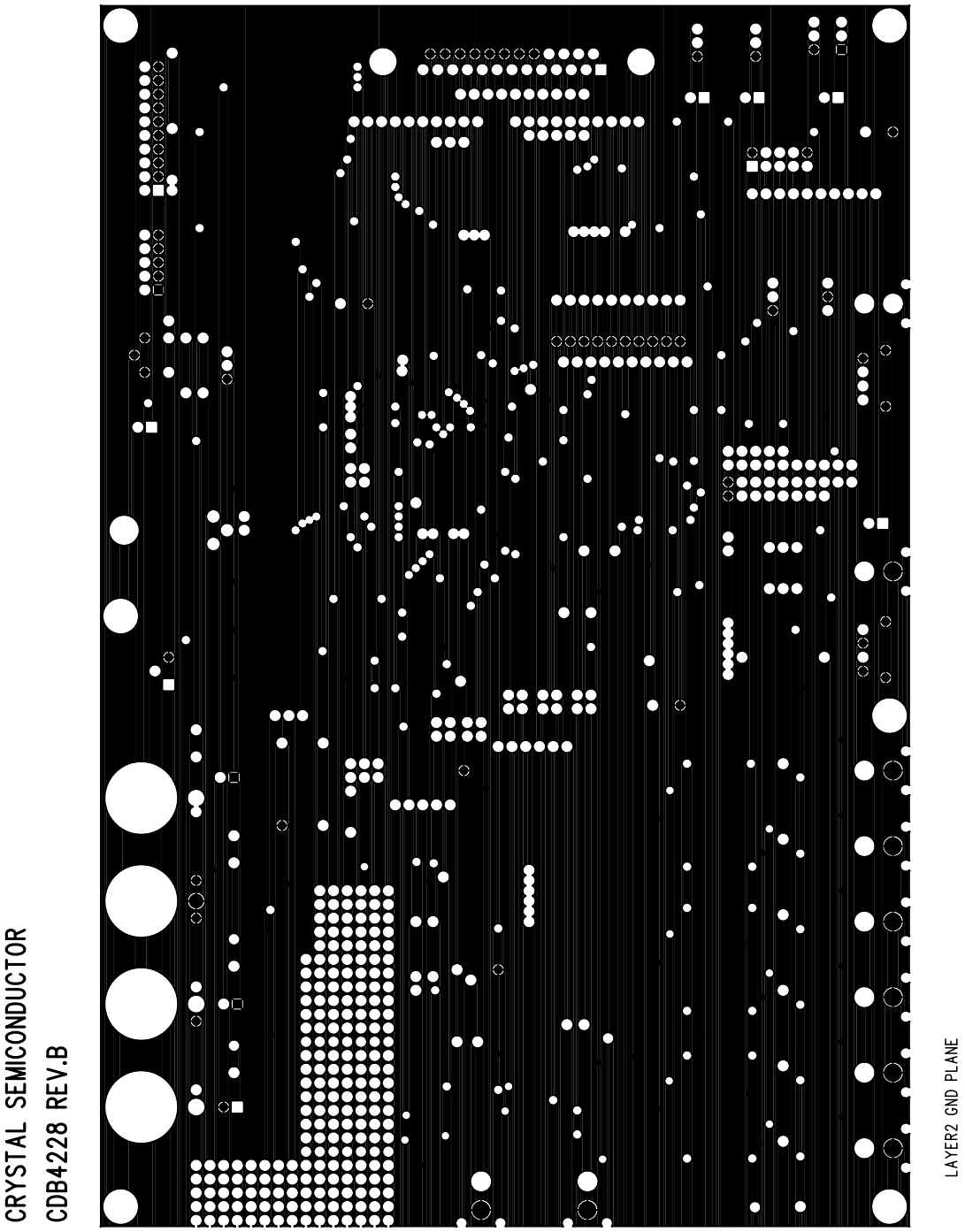

Figure 20. Level 2 Ground Plane

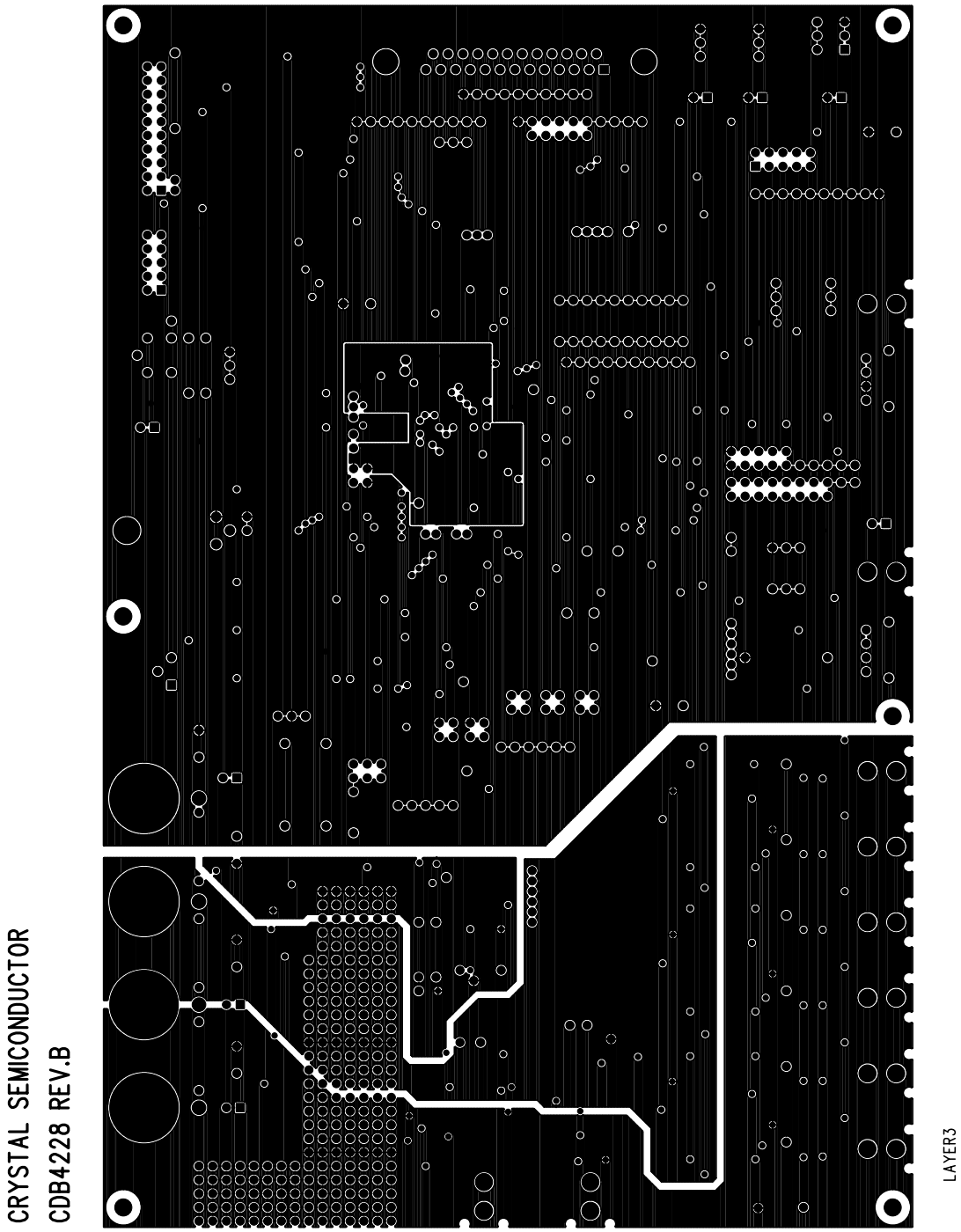

Figure 21. Level 3

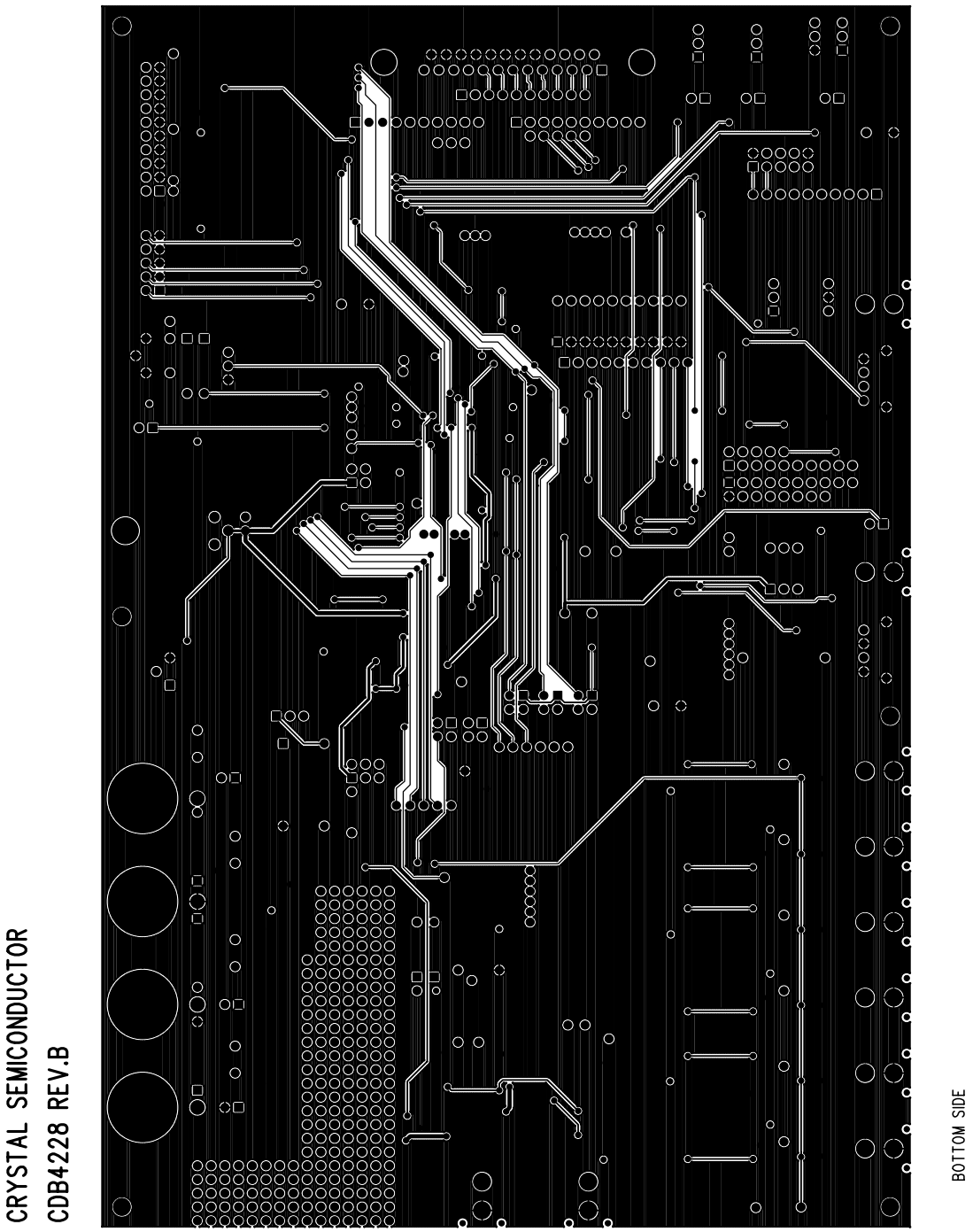

Figure 22. Bottom Side

10. BILL OF MATERIALS

Item	Qnty	Reference	Value	Mfg	Mfg P/N	Description	PCB Footprint
1	55	C1,C2,C3,C4,C6,C9,C12, C13,C15,C16,C17,C18,C27, C28,C29,C30,C31,C32,C34, C35,C39,C42,C44,C45,C46, C47,C49,C50,C51,C57,C60, C67,C70,C76,C77,C78,C79, C83,C85,C87,C88,C90,C100, C101,C103,C109,C111,C114, C115,C117,C118,C119,C120, C121,C122	47nf	KEMET	C1206C473K5RAC	CAP, CERAMIC, 47NF, 50V, 10%, X7R, 1206	CSN_1206
2	25	C5,C7,C8,C19,C20,C33,C40, C53,C58,C63,C68,C73,C84, C86,C89,C95,C96,C97,C98, C99,C104,C105,C106,C107,C108	10uf	PANA-SONIC	ECE-V1CS100SR	CAP, ELECT, 10UF, 16V, 20%, AL, SM_A	CSP_ELEC_130SQ
3	12	C38,C41,C52,C54,C56,C59, C62,C64,C66,C69,C72,C74	1nf	KEMET	C1206C102J1GAC	CAP, CERAMIC, 1NF, 100V, 5%, NPO, 1206	CSN_1206
4	10	C43,C55,C61,C65,C71,C75, C80,C81,C92,C93	100pf	KEMET	C1206C101J1GAC	CAP, CERAMIC, 100PF, 100V, 5%, NPO, 1206	CSN_1206
5	1	C48	68nf	KEMET	C1206C683K5RAC	CAP, CERAMIC, 68NF, 50V, 10%, X7R, 1206	CSN_1206
6	2	C82,C91	2.2nf	KEMET	C1206C222J1GAC	CAP, CERAMIC, 2.2NF, 50V, 5%, NPO, 1206	CSN_1206
7	6	C94,C102,C110,C112,C113,C116	22uf	PANA-SONIC	ECE-V1EA220SP	CAP, ELECT, 22UF, 25V, 20%, AL, SM_D	CSP_ELEC_260SQ
8	2	D2,D1	RED LED	LITEON	LT1139	LED, RED, DIFF, T1	LED_T-1
9	6	D3,D4,D5,D6,D7,D8	GREEN LED	LITEON	LT1142	LED, GREEN, DIFF, T1	LED_T-1
10	4	D9,D10,D14,D15	1N4148	LITEON	1N4148	DIODE, SWITCHING, DO35	DO35
11	2	D11,D12	P6KE13A	MOTOR-OLA	P6KE13A	DIODE, ZENER, 13V, DO7	DO7
12	1	D13	P6KE6.8A	MOTOR-OLA	P6KE6.8A	DIODE, ZENER, 6.8V, DO7	DO7
13	1	JP1	HDR3X1	SAMTEC	TSW-103-07-G-S	HEADER, MALE, 3X1	HDR3X1
14	1	JP2	HEADER 3X2	SAMTEC	TSW-103-07-G-D	HEADER, MALE, 3X2	HDR3X2
15	6	JP3,JP4,JP5,JP6,JP10,JP11	HEADER 2X2	SAMTEC	TSW-102-07-G-D	HEADER, MALE, 2X2	HDR2X2

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16	2	JP7,JP9	HEADER 5X2	SAMTEC	TSW-105-07-G-D	HEADER, MALE, 5X2	HDR5X2
17	1	JP8	HEADER 10X2	SAMTEC	TSW-110-07-G-D	HEADER, MALE, 10X2	HDR10X2
18	10	J1,J2,J7,J8,J9,J10,J11, J12,J13,J14	PHONO JACK RA	A/D ELECT	ARJ2018	PHONO JACK, RA, GOLD	CON_RCA_RA
19	1	J3	TERMI-NAL BLUE	E.F.JOHNSON	111-0110-001	BINDING POST, BLUE, BPOST	CON-BINDPOST
20	1	J4	TERMI-NAL BLACK	E.F.JOHNSON	111-0103-001	BINDING POST, BLACK, BPOST	CON-BINDPOST
21	1	J5	TERMI-NAL GREEN	E.F.JOHNSON	111-0104-001	BINDING POST, GREEN, BPOST	CON-BINDPOST
22	1	J6	TERMI-NAL RED	E.F.JOHNSON	111-0102-001	BINDING POST, RED, BPOST	CON-BINDPOST
23	1	J15	DB25M_RA	ADAM TECH	DB25-PL-24	CONNECTOR, DB25, MALE, RA	CON_DB25M_RA
24	5	L1,L3,L4,L5,L6	ELDR25	PANA-SONIC	EXC-ELDR25	FERRITE, RADIAL, RADIAL200	EXC-ELDR25
25	1	L2	47uH	J.W. MILLER	8230-60	INDUCTOR, 47UH, SHIELDED, IND500	IND500
26	6	Q1,Q2,Q3,Q4,Q5,Q6	2SC3326	TOSHIBA	2SC3326	BJT, NPN, MUTE, SC59	SC59
27	1	Q7	MUN2111T1	MOTOR-OLA	MUN2111T1	BJT, PNP, 10K INTERNAL BIAS, SC59	SC59
28	1	Q8	MUN2211T1	MOTOR-OLA	MUN2211T1	BJT, NPN, 10K INTERNAL BIAS, SC59	SC59
29	3	RP1,RP2,RP10	10k RPACK9	BOURNS	4610X-101-103	RES, R-PACK9, 10K, 1/8W, 2%, SIP10	SIP10
30	4	RP3,RP4,RP5,RP8	1k RPACK9	BOURNS	4610X-101-102	RES, RPACK9, 1K, 1/8W, 2%, SIP10	SIP10
31	2	RP7,RP6	4.7k RPACK8	BOURNS	4816P-T01-472	RES, RPACK8, 4.7K, 1/8W, 2%, SOM16	SO16-220
32	1	RP9	22 RPACK8	BOURNS	4816P-T01-220	RES, RPACK8, 22, 1/8W, 2%, SOM16	SO16-220
33	15	R1,R2,R4,R22,R23,R24,R25, R66,R67,R68,R69,R70,R71, R72,R73	33	PANA-SONIC	ERJ-8GEYJ330	RES, THICK FILM, 33, 1/8W, 5%, 1206	RES_1206

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34	3	R3,R94,R95	0	YAGEO	ERJ-8GEYJ000	RES, 0 OHM JUMPER, 1/8W, 1206	RES_1206
35	13	R5,R7,R20,R74,R77,R78, R79,R81,R84,R85,R86,R96,R97	10k	PANA-SONIC	ERJ-8ENF1002	RES, THICK FILM, 10K, 1/8W, 1%, 1206	RES_1206
36	25	R6,R13,R14,R17,R18,R27, R28,R31,R33,R34,R35,R38, R39,R45,R46,R49,R51,R52, R53,R56,R57,R59,R60,R63,R65	3.16k	PANA-SONIC	ERJ-8ENF3161	RES, THICK FILM, 3.16K, 1/8W, 1%, 1206	RES_1206
37	2	R8,R82	8.25k	PANA-SONIC	ERJ-8ENF8251	RES, THICK FILM, 8.25K, 1/8W, 1%, 1206	RES_1206
38	7	R9,R11,R12,R42,R43,R44,R91	374	PANA-SONIC	ERJ-8ENF3740	RES, THICK FILM, 374, 1/8W, 1%, 1206	RES_1206
39	1	R10	93.1	PANA-SONIC	ERJ-8ENF93R1	RES, THICK FILM, 93.1, 1/8W 1%, 1206	RES_1206
40	6	R15,R29,R36,R47,R54,R61	604	PANA-SONIC	ERJ-8ENF6040	RES, THICK FILM, 604, 1/8W, 1%, 1206	RES_1206
41	6	R16,R30,R37,R48,R55,R62	100k	PANA-SONIC	ERJ-8GEYJ104	RES, THICK FILM, 100K, 1/8W, 5%, 1206	RES_1206
42	6	R19,R32,R40,R50,R58,R64	1.78k	PANA-SONIC	ERJ-8ENF1781	RES, THICK FILM, 1.78K, 1/8W, 1%, 1206	RES_1206
43	1	R21	470	PANA-SONIC	ERJ-8GEYJ470	RES, THICK FILM, 470, 1/8W, 5%, 1206	RES_1206
44	4	R26,R104,R105,R106	75	PANA-SONIC	ERJ-8ENF75R0	RES, THICK FILM, 75, 1/8W, 1%, 1206	RES_1206
45	1	R41	33k	PANA-SONIC	ERJ-8GEYJ333	RES, THICK FILM, 33K, 1/8W, 5%, 1206	RES_1206
46	10	R75,R80,R83,R88,R98,R99, R100,R101,R102,R103	150	PANA-SONIC	ERJ-8ENF1500	RES, THICK FILM, 150, 1/8W, 1%, 1206	RES_1206
47	2	R76,R87	4.99k	PANA-SONIC	ERJ-8ENF4991	RES, THICK FILM, 4.99K, 1/8W, 1%, 1206	RES_1206
48	2	R89,R90	1k	PANA-SONIC	ERJ-8GEYJ102	RES, THICK FILM, 1K, 1/8W, 5%, 1206	RES_1206
49	1	R92	121	PANA-SONIC	ERJ-8ENF1210	RES, THICK FILM, 121, 1/8W, 1%, 1206	RES_1206
50	1	R93	500 POT	BOURNS	3296Y-501	POTENTIOMETER, 25T, TOP ADJ, 500, 3296Y	POT_BRNS_3296Y
51	1	S1	SW DIP-3	GRAYHILL	76SB03	SWITCH, DIP, 3 POS, ROCKER, DIP6	SW-DIP3
52	2	S3,S2	SW SPDT	C&K	TS01CBE	SWITCH, SLIDE, SPDT	SW_CK_TS01CBE
53	1	S4	SW DPDT	AUGUAT	TSS21NGPC	SWITCH, SLIDE, DPDT	SW_AGT_TSS21NGPC

Table 6. Bill of Materials

54	1	S5	PTS645 TL50	C&K	PTS645TL50	SWITCH, 6MM TACT W/ ESD PIN, 130GF, DPST	SW-MOM-C&K
55	1	S6	SW DIP10	GRAYHILL	76SB10	SWITCH, DIP, 10 POS, ROCKER, DIP20	SW-DIP10
56	106	TP1,TP2,TP3,TP4,TP5,TP6,TP7, TP8,TP9,TP10,TP11,TP12,TP13, TP14,TP15,TP16,TP17,TP18, TP19,TP20,TP21,TP22,TP23, TP24,TP25,TP26,TP27,TP28, TP29,TP30,TP31,TP32,TP33, TP34,TP35,TP36,TP37,TP38, TP39,TP40,TP41,TP43,TP47, TP48,TP49,TP50,TP51,TP53, TP55,TP56,TP58,TP60,TP61, TP64,TP65,TP66,TP67,TP68, TP69,TP70,TP71,TP72,TP73, TP74,TP75,TP76,TP77,TP78, TP79,TP80,TP81,TP82,TP83, TP84,TP85,TP86,TP87,TP88, TP89,TP90,TP91,TP92,TP93, TP94,TP95,TP96,TP97,TP98, TP99,TP100,TP101,TP102, TP103,TP104,TP105,TP106, TP107,TP108,TP109,TP110, TP111,TP112,TP113,TP114, TP115,TP116	TEST POINT	-	-	TEST POINT, PAD60R40	TESTPOINT
57	1	T1	67129600	SCHOTT	67129600	XFMR, PULSE, TH	XFR_SC67129600
58	1	U1	12.2880 MHZ	CAL CRYSTAL	CX21AF-12.2880MHZ	IC, OSCILLATOR, 12.2880MHZ, 50PPM, OSC14	OSC-FULL
59	1	U2	74AC125SC	FAIR-CHILD	74AC125SC	IC, TRISTATE BUFFER, QUAD, SO14	SO14-150
60	1	U3	CS4228A-KS	CRYSTAL	CS4228D-KS	IC, CODEC, SSOP28	SSOP28-209
61	1	U4	CS8404A-CS	CRYSTAL	CS8404A-CS	IC, SPDIF TX, SOIC24	SO24-300
62	1	U5	TOTX173	TOSHIBA	TOTX173	IC, OPTICAL TXMTR	TOTX173
63	1	U6	EPM7128STC100-15	ALTERA	EPM7128STC100-15	IC, CPLD, 128MC, 15NS, TQFP100	QFP100_14X14
64	5	U7,U10,U11,U14,U15	MC33078	MOTOR-OLA	MC33078D	IC, OPAMP, DUAL, SO8	SO8-150

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65	1	U8	CS8414-CS	CRYSTAL	CS8414-CS	IC, SPDIF RX, SOIC28	SO28-300
66	1	U9	TORX173	TOSHIBA	TORX173	IC, OPTICAL RX	TORX173
67	2	U13,U12	74HC245AWM	FAIR-CHILD	MM74HC245AWM	IC, TRANCEIVER, HEX, SOW20	SO20-300
68	1	U16	LT1086CT-3.3	LINEAR	LT1086CT-3.3	IC, VOLTAGE REG, POSITIVE, 3.3V, TO220	TO-220AB
69	1	U17	DS1233-10	DALLAS	DS1233-10	IC, POWER SUPPLY MONITOR, TO92	TO-92
100	4	U1		AUGUAT	8134-HC-5P2	SOCKET, PIN, POP-IN, SM	
101	6	-		Key-stone/DK	8401K-ND	1/2" X 4-40 HEX STANDOFF	
102	6	-		MCMAS-TER CARR	91773A108/PAN4CR6SZ	4-40 3/8" MACHINE SCREW, PAN	
103	4	-		MOLEX	15-29-1025	SHUNT, OPEN END	
104	4	J3,4,5,6				Connect wire, 20GA, Stranded, 2"	
105	3	JP6, 10, 11				shorting jumper, 22GA, solid	
106	2	J15				MACHINE SCREW, 6-32 x 1/2", PAN HEAD	
107	2	J15				NUT, #6	

Table 6. Bill of Materials


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